What is claimed is :

1. A phase comparator provided in a phase locked loop circuit, said phase comparator converting a phase difference between first and second input signals into a current signal,

wherein said phase comparator has :

a lock detector for detecting locked and unlocked states of said phase locked loop circuit to generate a detected signal which indicates one of said locked and unlocked states ; and

a current source connected to said lock detector for receiving said detected signal from said lock detector and varying a supply current based on said detected signal, so that if said detected signal indicates said unlocked states, then said current source increases said supplying current.

2. The phase comparator as claimed in claim 1, wherein if said detected signal indicates said locked states, then said current source decreases said supplying current.

3. The phase comparator as claimed in claim 2, wherein said current source comprises a pair of a constant current source for supplying a constant current and a variable current source connected to said lock detector for varying a current based on said detected signal.

4. The phase comparator as claimed in claim 3, wherein said lock

detector is connected between an output terminal of said phase comparator and said variable current source.

5. The phase comparator as claimed in claim 4, wherein said phase comparator includes plural current mirror circuits.

6. The phase comparator as claimed in claim 5, wherein each of said plural current mirror circuits comprises a pair of bipolar transistors.

7. The phase comparator as claimed in claim 6, wherein a base current compensating bipolar transistor is connected to one of said paired bipolar transistors of each of said plural current mirror circuits.

8. The phase comparator as claimed in claim 7, wherein said base current compensating bipolar transistor has a base connected to a collector of said one of said paired bipolar transistors, and an emitter connected to a base of said one of said paired bipolar transistors.

9. A phase locked loop circuit comprising :

an input terminal ;

an output terminal ;

a phase comparator connected to said input terminal ;

a loop filter connected to said phase comparator ;

a voltage controlled oscillator connected to said loop filter, and

said voltage controlled oscillator connected to said output terminal ;

a mixer connected to said output terminal and also connected to said phase comparator, so that said phase comparator receives a first input signal from said input terminal and a second input signal from said mixer for converting a phase difference between said first and second input signals into a current signal,

wherein said phase comparator has :

a lock detector for detecting locked and unlocked states of said phase locked loop circuit to generate a detected signal which indicates one of said locked and unlocked states ; and

a current source connected to said lock detector for receiving said detected signal from said lock detector and varying a supply current based on said detected signal, so that if said detected signal indicates said unlocked states, then said current source increases said supplying current.

10. The phase locked loop circuit as claimed in claim 9, wherein if said detected signal indicates said locked states, then said current source decreases said supplying current.

11. The phase locked loop circuit as claimed in claim 10, wherein said current source comprises a pair of a constant current source for supplying a constant current and a variable current source connected to said lock detector for varying a current based on said detected signal.

12. The phase locked loop circuit as claimed in claim 11, wherein said lock detector is connected between an output terminal of said phase comparator and said variable current source.

13. The phase locked loop circuit as claimed in claim 12, wherein said phase comparator includes plural current mirror circuits.

14. The phase locked loop circuit as claimed in claim 13, wherein each of said plural current mirror circuits comprises a pair of bipolar transistors.

15. The phase locked loop circuit as claimed in claim 14, wherein a base current compensating bipolar transistor is connected to one of said paired bipolar transistors of each of said plural current mirror circuits.

16. The phase locked loop circuit as claimed in claim 15, wherein said base current compensating bipolar transistor has a base connected to a collector of said one of said paired bipolar transistors, and an emitter connected to a base of said one of said paired bipolar transistors.

17. A method of phase comparison in a phase locked loop circuit by converting a phase difference between first and second input signals into a current signal, said method comprising the steps of :

detecting locked and unlocked states of said phase locked loop

circuit to generate a detected signal which indicates one of said locked and unlocked states ; and

varying a supply current based on said detected signal, so that if said detected signal indicates said unlocked states, then said supplying current is increased.

18. The method as claimed in claim 17, wherein if said detected signal indicates said locked states, then said supplying current is decreased.